Ethan Gabizon

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Education

Cornell University, College of Engineering Expected May 2025
B.S., Electrical & Computer Engineering *Current GPA: 3.7/4.0*

Relevant Coursework

Courses: Compilers, Advanced Computer Architecture, Digital VLSI Design, Programming Languages, Data Structures & Functional Programming, Data Structures & OOP

Skills

Languages: Verilog/SystemVerilog, Rust, Java, C, OCaml, Tcl, Python, x86 assembly, Arm assembly
Tools: Git/GitHub, Unix Shell, Linux, VS Code, AMD Vitis/Vivado, Intel Quartus, Cadence Virtuoso

Experience

Cornell Capra Lab | Undergraduate Researcher May 2023 – Present
- Contributing to Filament, a novel hardware description language and compiler that uses a type system to ensure correctness and efficiency in pipelined hardware designs
- Architected a RISC-V processor in Filament capable of running programs with the 32I ISA
- Implemented parametric BLAS kernels and evaluated resource usage on Xilinx FPGAs
- Implemented monomorphization & multiple type-checking passes in Filament's compiler to identify structural errors at compile-time and report helpful error messages
- Authored 8,000+ lines of code across compiler passes, test suites, and hardware designs written in Filament
- Benchmarked Filament designs based resource usage, throughput, and clock frequency using Vivado synthesis tools
- Co-authored a paper on Filament. Revising for submission to PLDI 2025

Cornell Custom Silicon Systems | Digital Subteam Member September 2022 – December 2023
- Worked with a small team to incrementally develop & test an SPI module in SystemVerilog
- Deployed SPI module on an FPGA for testing with real I/O
- Coordinated with teams developing other modules to perform integration testing

Cornell College of Engineering | Teaching Assistant August 2022 – Present
- Led lab sessions and office hours for ECE 2300: Digital Logic and ECE 4750: Computer Architecture
- Prepared and delivered lectures about computer architecture and Verilog design
- Helped students understand concepts including FSMs, timing analysis, multi-core processor architecture, memory hierarchy out-of-order processing, and branch prediction
- Developed lab assignments where students design, implement, and test a multi-core RISC-V processor

Cornell Computer Systems Lab | Undergraduate Researcher June 2022 – January 2023
- Contributed to IMpress, an FPGA resource optimizer for cryptographic algorithms
- Used Vivado HLS to synthesize and optimize large adders and multipliers for the IMpress library
- Designed comprehensive test benches to verify functionality and characterize latency of arithmetic units
- Wrote Tcl scripts to sweep parameters (bit width, latency, resource type) of Xilinx IP Cores
- Wrote Python scripts to extract resource usage & timing information from HLS reports

Projects

Optimizing Compiler January 2023 – May 2023
- Developed an x86-targeted compiler a C-like imperative language, including lexing, parsing, and type-checking
- Designed an AST and intermediate representation for the language, enabling optimization passes
- Implemented register allocation & copy propagation using dataflow analysis

Multicore RISC-V Processor August 2023 – December 2023
- Designed and implemented quad-core fully-bypassed RISC-V processor at the register-transfer level
- Integrated core with an associative cache and ring network to run parallel C programs
- Verified all subcomponents by achieving 90-100% toggle coverage, ensuring correctness of overall design
- Achieved a 3.7× speedup over single-core system for multi-threaded sorting benchmarks